

Silicon and Silicon-dioxide Processing for High-frequency MESFET Preparation*

Abstract: Silicon wafer processing is described which provides submicrometer epitaxial layers on top of high-resistivity silicon substrates for fabrication of high-frequency metal-semiconductor field-effect transistors. Silicon-dioxide underetching at the border of an oxide window, performed in hydrogen at elevated temperatures, is one method of realizing 1-micrometer device structures.

Semiconductor devices for operation in the gigahertz range are of interest in many fields of electronics—for example, in communication, data transmission and switching. Field-effect transistors with Schottky gates (MESFET's)[†] show promise of suitable properties.¹ The main problems in such high-frequency devices arise especially from the following requirements: a) The substrate has to be of high resistivity to prevent parasitic capacitances and to separate devices from one another; the technology with p-type substrates and p-type frame diffusion as used for isolation purposes in n-channel devices is no longer applicable due to high parasitic contributions. b) The channel layer has to be very thin, of specified doping concentration and high carrier mobility to realize devices of high transconductance. Reproducibility and layer uniformity are problems in the deposition of layers of 0.2 micrometer thickness, which is smaller by about a factor of ten than are deposits commonly prepared by epitaxy. c) The device geometry has to be very small to realize intrinsic high-frequency properties. This latter problem arises from the usual limits of photo-masking which one normally does with a few micrometers of line width or separation. A particularly serious difficulty here is the realignment of successive masks. For very small structures there was a strong need for new masking schemes.

Approach

The approach chosen to fulfill these requirements will be outlined in detail in the next section. Its main characteristics are:

- a) A substrate of slightly doped p-type silicon, having increased resistivity as a result of elevated temperature processing;
- b) A channel layer prepared by silicon epitaxy at low temperatures and deposition rates. The layer could be obtained as a continuous film or as a deposit on pre-selected areas;
- c) A 1 μm gate length realized by reduction of the geometrical dimensions by silicon dioxide underetching at the border of a window.

Procedures and results

• High-resistivity silicon substrate

The utilization of silicon as a substrate material of high resistivity is a compromise, since its insulating quality is not ideal and since changes in electrical properties do occur during wafer processing.^{2,3} Nevertheless, it is preferable to the silicon-on-sapphire or other hetero-

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[†] MESFET is the acronym for Metal-Semiconductor Field-Effect Transistor.

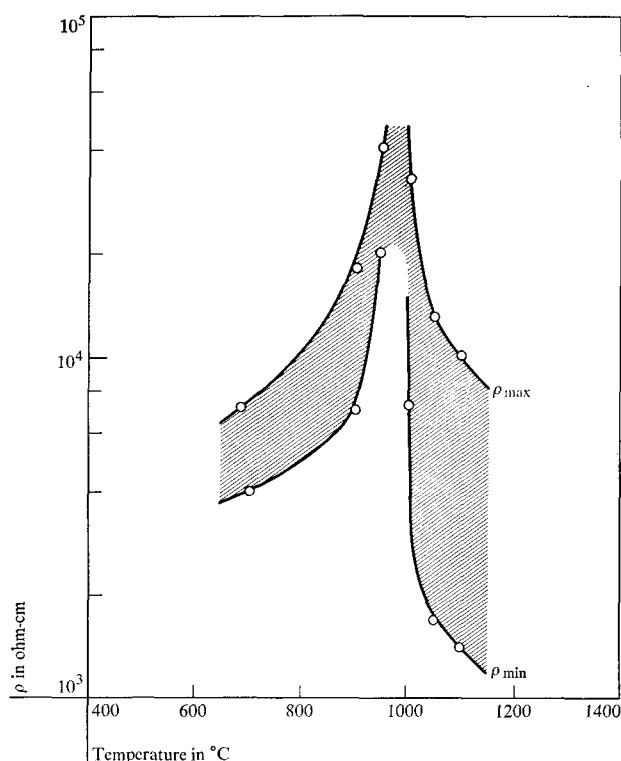


Figure 1 Resistivity ρ as a function of annealing temperature.

epitaxial approaches where, due to the nucleation process, it is difficult to realize very thin ($0.2 \mu\text{m}$ or less) epitaxial layers of high crystallographic perfection and high electrical quality.

Recently, P. Richman² reported the application of high-resistivity p-type silicon substrates in complementary MOS-FET arrays. For p-type substrates with a resistivity ρ higher than $10,000 \text{ ohm-cm}$, no deterioration in the rectifying properties of junctions formed with p^+ (or n^+) silicon were found when all the diffusion and oxidation temperatures were kept below 1100°C . For silicon with lower resistivities, conversion to n-type was observed in some of the experiments. The material used in this work was a floating zone refined p-type silicon of $2,000\text{--}3,000 \text{ ohm-cm}$. It was found that during heat treatment up to 950°C , the resistivity increases by about one order of magnitude, reaching values as high as 50 kohm-cm . In excess of about 950°C the resistivity then drops as the material converts to n-type. The temperature dependence of resistivity as measured by the four-point probe method is shown in Fig. 1. The n-doping component was not identified. It may come from inside the material, or from fast diffusers. Hydrogen or oxygen atmospheres provided similar results. Annealing time was found to be of little influence. The change in resistivity after a 5-minute

heat-treatment at 950°C was about the same as after an additional 2 hours. This behavior simplifies wafer processing, because temperature is the only significant parameter. It should not exceed 950°C during all the processing steps. Temperature cycles up to 550°C (as utilized for ohmic contact preparation) did not reduce the resistivity below 10 kohm-cm . The reported resistivity behavior of our substrate material is in qualitative agreement with the observations of B. Victoria,³ who studied aging effects on annealed high-resistivity p-type silicon ($1,800\text{--}3,400 \text{ ohm-cm}$). From his and our own observations it can be expected that long-time or even elevated-temperature storage does not reduce the resistivity below the value before annealing.

Advantageous use of the high-resistivity substrate was demonstrated in experiments on $4 \mu\text{m}$ gate length transistors, performed together with P. Wolf. The geometrical layout used was the same as described by H. Statz and W. v. Münch⁴ and shown in Fig. 2 for the extreme cases. Table 1 summarizes the important parameters of the three structures under consideration. The results of source-gate and drain-gate capacitance measurements as obtained with a Boonton three-terminal bridge are shown in Table 2. The operating conditions are given in the footnote.

There is satisfactory agreement between the measured and calculated capacitances. The decrease in parasitics in going from structure a) to structure c) is considerable. It demonstrates the practical value of the high-resistivity substrate.

•Channel layer preparation by thin film epitaxy

Silicon epitaxy by hydrogen reduction of silicon tetrachloride was utilized to prepare the active channel layer of the device. At 950°C substrate temperature, a deposition rate of 400 to 600 Å/min was found to be slow enough to obtain reproducibly uniform layers of $0.2 \mu\text{m}$ thickness in a horizontal flow reactor. The n-doping was accomplished by admission of AsH_3 to the main hydrogen gas-flow of 12 l/min . To be accurate enough in the deposited layer thickness ($\pm 10\%$) and doping concentration ($\pm 10\%$) two or three epitaxial preruns were performed to calibrate the equipment. In all the following runs one wafer was examined by optical interference and the four-point probe method for additional adjustment of thickness and doping. The Si epitaxial process was successfully employed either for the deposition of continuous films over a whole wafer or for deposition onto selected areas of Si substrates defined by windows in the oxide.

To investigate crystallographic layer quality, continuous deposits of 3 to $4 \mu\text{m}$ thickness were grown on silicon of very low dislocation density. It was found by preferential etching⁵ that for clean experimental conditions in a few runs no extra dislocations were formed in the deposit, while the number of stacking faults amounted to less than $2,000 \text{ per cm}^2$. The results of experiments to deter-

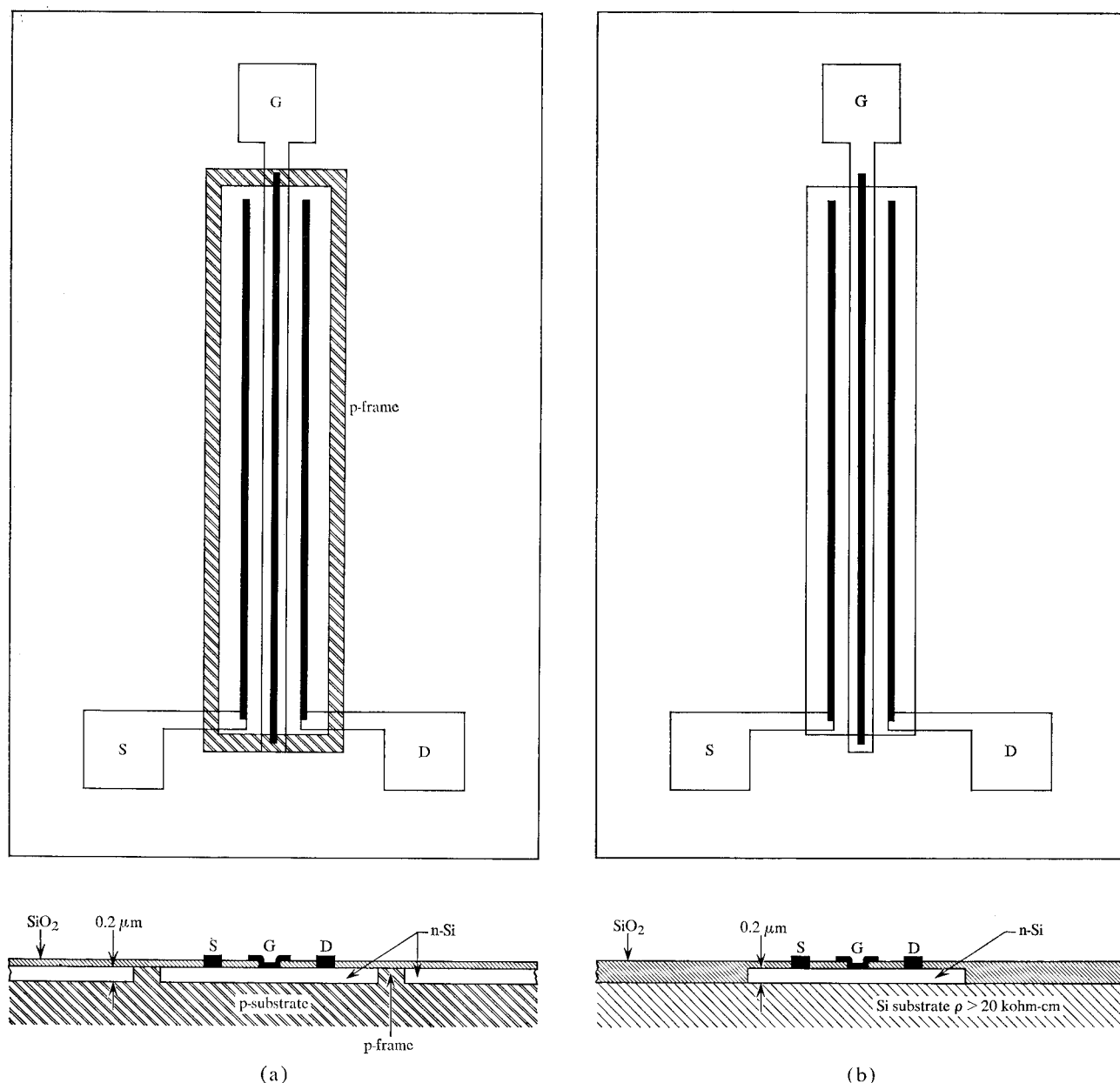


Figure 2 a) Device structure "a" of Table 1 with pn-junctions. b) Device structure "c" of Table 1, free of pn-junctions.

mine the dislocation density and stacking-fault density as a function of the deposition temperature are shown in Table 3. The growth rate of the epitaxial layer was kept constant within 20% of 400 Å/min by suitable adjustment of the temperature of the SiCl₄ bath. The low density of faults can be understood as a result of in situ surface cleaning, which occurred during the heating-up period and the 2 minute stabilization period at maximum temperature, before epitaxy was started. From the observation of slight silicon removal in the case of selective epitaxy, it might be concluded that surface cleaning by silicon etching was due to the presence of oxide lands (for thickness

measurement) on all the wafers, and the formation of sufficient water vapor. The electrical quality of the layer was determined by Hall mobility measurements. For films down to 0.15 μm thickness and a doping concentration in the range of 10¹⁷ per cm³, the deviation from bulk material mobility data as measured in the same setup was less than ± 10% in most cases. The results obtained are shown in Fig. 3.

• Device structure

For improving the high-frequency behavior of a device, the gate length (direction of current flow) should be made

Table 1 Summary of important parameters for three transistor structures with and without pn-junctions.

Structure a)

10 Ohm-cm p-type silicon substrate, p-frame diffusion, continuous n-layer (Fig. 2a)

Structure b)

High-resistivity substrate, p-frame diffusion, continuous n-layer

Structure c)

High-resistivity substrate, no p-frame, n-layer only in the active device area (Fig. 2b)

Gate length	4 μm
Gate extension	250 μm
Thickness of the channel	0.2 to 0.3 μm
Distance between source and drain	22 μm
Doping concentration in the channel	0.5 to $1.0 \times 10^{17} \text{ cm}^{-3}$

Table 2 Source-gate and drain-gate capacitances, in pF, for the three transistor structures of Table 1, with given operating conditions.*

	Structure a)	Structure b)	Structure c)
Measured source-gate capacitance	1.32	0.55	0.35
Calculated	1.39 1.17 paras.	0.40 0.18 paras.	0.27 0.05 paras.
Measured drain-gate capacitance	0.51	0.35	0.17
Calculated	0.64 0.61 paras.	0.25 0.22 paras.	0.13 0.10 paras.

* Operating conditions;

Source-gate bias voltage

Source-drain bias voltage (to achieve drain current saturation)

Measurement frequency

$V_{sg} = 0$

$V_{sd} = 5\text{V}$

1 MHz

Table 3 Dislocation density and stacking fault density in silicon epilayers for deposition temperatures between 900° and 1000°C.

Deposition temperature (°C)	Dislocation density (cm^{-2})	Stacking fault density (cm^{-2})
900	2200	2500
950	1900	1800
975	1200	1100
1000	600	700

Within 1 mm of the wafer periphery the number of faults was higher by about one order of magnitude.

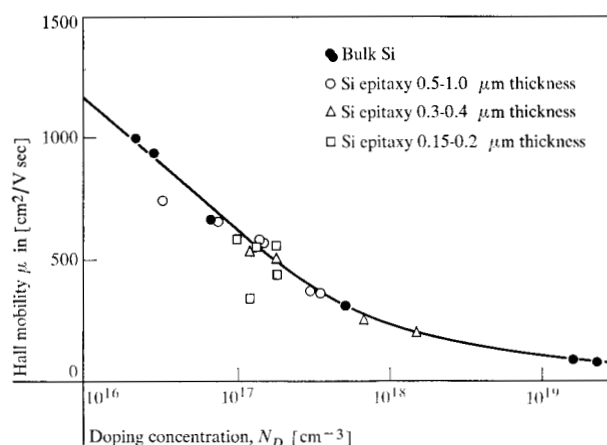
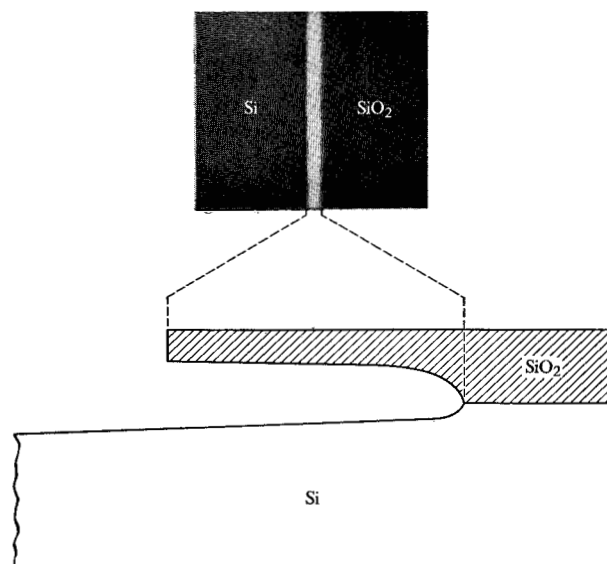


Figure 3 Hall mobility versus doping concentration as measured for bulk material and epitaxial layers below 1 μm thickness.

Figure 4 Underetched silicon dioxide, photograph (2.5 μm wide) and cross section.



as short as possible, since it is a significant parameter in increasing transconductance and decreasing capacitance. A desirable and attainable gate length and contact separation distance seemed to us to be one micrometer. Difficulties concerned with this small structure were overcome with two different techniques, both of which have been used successfully. They have in common the high-resistivity substrate and the thin epitaxial layer. One technique realizes the transistor pattern with 1- μm dimensions by projection masking in conjunction with gold spreading, as described by S. Middelhoeck.^{6,7} The transistor with a maximum oscillation frequency of 12 GHz was made in

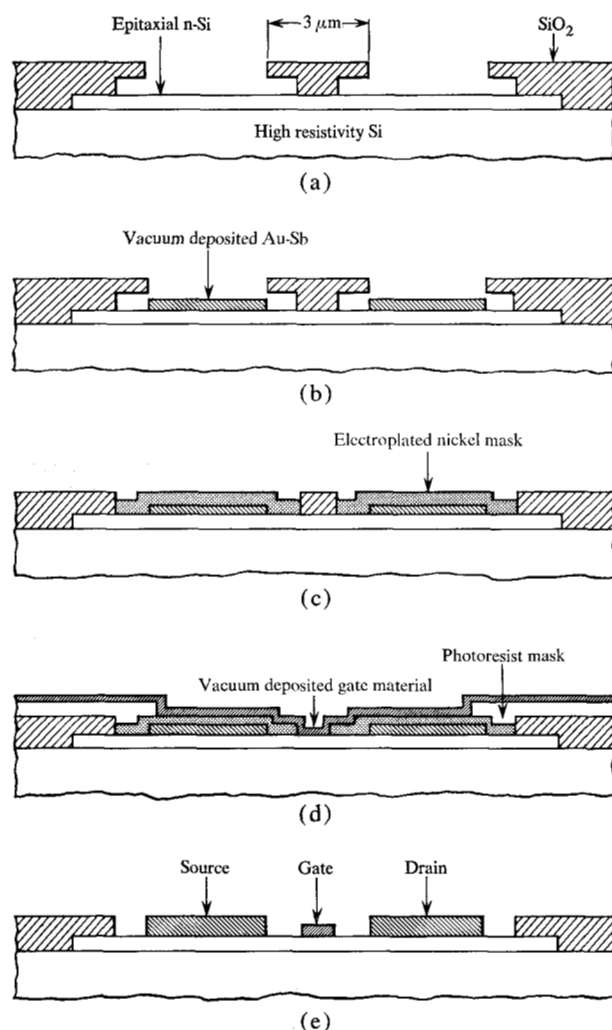
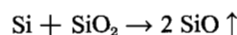


Figure 5 Processing steps of a MESFET prepared by the SiO_2 underetching method. (See text).

this way. The other technique, which is more flexible in the choice of the gate material, utilizes oxide underetching at the border of a window to reduce the geometrical dimensions of an oxide strip in contact with silicon, and to accomplish self-registration for the gate. Underetching of silicon dioxide in contact with silicon, as shown in Fig. 4, is obtained by annealing the wafer in hydrogen at elevated temperatures, for example, at 950°C . For an oxide of $0.2\ \mu\text{m}$ thickness, prepared by the dry-wet-dry process, a distance of underetching up to $4\ \mu\text{m}$ was realized. The amount of vertical silicon and oxide etching was comparably small. For the etched-off silicon, a depth of about $300\ \text{\AA}$ was measured by optical interference.

The strong difference between the horizontal and vertical etch rates at the border of a window in the oxide (directions in respect to the surface of the wafer) may be due to the following:

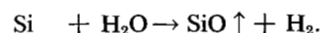
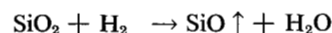
1) A direct reaction between silicon and silicon dioxide according to the equation⁸



and the possibility of SiO evaporation along the edge of the window. The reaction in the vertical direction stops as the contact between silicon and silicon dioxide is interrupted.

2) The existence of an inherent ease of etching of the oxide at the Si-SiO_2 interface. This oxide property may arise from the preparation procedure (incorporated OH from the dry-wet-dry process), from an oxygen concentration gradient, or from built-in stresses at the Si-SiO_2 interface.

3) Low vertical silicon etch rates within the underetched region as a result of the low mean free path (and therefore reduced mass transport) for H_2O molecules. The H_2O molecule formed at the SiO_2 surface is an important agent in the reaction described by the general equations⁸



The etch rate in the horizontal direction is not reduced by mean-free-path effects because of the close vicinity of silicon and silicon dioxide at the released interface.

Experiments with different qualities of oxide and different conditions for underetching are being carried out to clarify the situation. The results will be published later in a separate paper. A practical application of oxide underetching is shown in Fig. 5.

To obtain the structure in Fig. 5a, n-type silicon is deposited onto the wafer by continuous or selective epitaxy. The layer is about $0.2\ \mu\text{m}$ thick and has a doping concentration of about $10^{17}/\text{cm}^3$. After oxidation by the dry-wet-dry process, conventional contact masking is applied to define about 500 double windows on the wafer, which later act as the contact areas of source and drain. The separation between the windows within one pair is $3\ \mu\text{m}$. They are etched into the oxide by chemical means. The next operation is oxide underetching. It is accomplished by annealing the wafer in hydrogen at 950°C , $1\ \mu\text{m}$ of underetching being obtained after 13 minutes. The lateral extension of the gate was usually $500\ \mu\text{m}$. Oxide underetching did not restrict this dimension. It was kept short because of the gate resistance, which has to be low for high-frequency performance of the device.

Figure 5b shows the situation after vacuum deposition of Au-Sb at 550°C . At this wafer temperature the gold alloys with the silicon and forms the ohmic contacts for source and drain. The underetched oxide frame acts as a well-registered mask and defines the separation distance between source-gate and drain-gate. The Au-Sb on top of the oxide is wiped off.

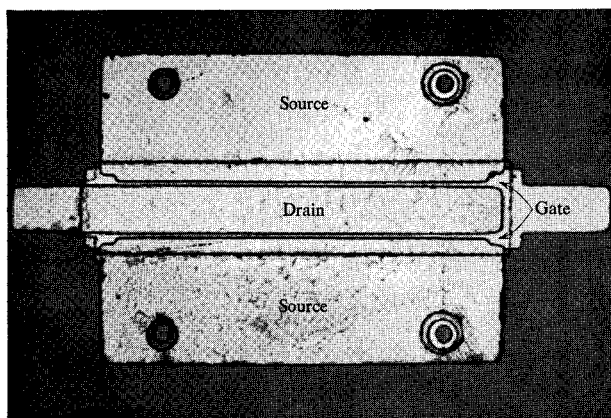


Figure 6 Photograph of a completed MESFET of 1- μm gate width and $2 \times 230 \mu\text{m}$ active length.

In Fig. 5c the underetched oxide frame is removed by short etching in buffered hydrofluoric acid. A layer of electroplated nickel is deposited over all the conducting area. With this masking step the position, length and extension of the gate is defined as the one-micrometer wide oxide strip still in contact with the silicon.

Gate formation is the main purpose of the following processing steps. The need of a contact land (not shown in cross section) requires a coarse photomask, as indicated in Fig. 5d by the wide opening in the gate region. As a next step all unmasked oxide is etched off in buffered hydrofluoric acid exposing the silicon, which has to be covered with gate material to the ambient. In the following step the gate material, which might be Cr-Au for example, is vacuum deposited over the entire wafer.

To obtain the final device structure as shown in Fig. 5e all Cr-Au except the gate itself is removed in two steps. It is lifted off after the photoresist underneath is dissolved in acetone and the nickel etched off in iron chloride. To reduce the resistance along the gate contact especially, pure gold is deposited by electroplating.

In a last processing step the devices are mounted on T0-46 headers. Figure 6 is a photograph of one configura-

tion of a MESFET taken before wire bonding. The device has two symmetrical sources and gates and a common drain.

The electrical measurements described in a paper by P. Wolf⁹ have shown for these devices a maximum transconductance of 40 mA/V per mm length and a maximum frequency of oscillation of 9 GHz. These properties are close to the optimum data reported.

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